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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,710	07/15/2003	Koichiro Ishibashi	1687.1004	4927

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,710	ISHIBASHI ET AL.	
	Examin r	Art Unit	
	Tu-Tu Ho	2818	

-- Th MAILING DATE of this communication appears on the cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15-26 and 30* is/are rejected.

7)☒ Claim(s) *12-14,16 and 27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/15/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/15/2003 is acceptable.

Claim Objections

2. Dependent claim 25 refers to a "said first diode" and a "said second diode". However, independent **claim 16**, on which claim 25 depends, simply refers a "diode" twice. Change "diode" on line 18 of claim 16 to "first diode" and change "diode" on line 23 of claim 16 to "second diode".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1 and 10-11** are rejected under 35 U.S.C. 102(b) as being anticipated by Dabral U.S. Patent 6,515,534 (hereinafter referred to as the '534 patent, which has a publication priority date of 06/13/2002).

The '534 patent discloses in Figures 3A and 3B and respective portions of the specification a semiconductor integrated circuit device as claimed.

Referring to **claim 1**, the '534 patent discloses a semiconductor integrated circuit device comprising:

a MISFET 310, having a source electrode 311 and a drain electrode of a first conductivity type and a gate electrode, formed in a well of a second conductivity type; and

a body biasing circuit 320 that generates a voltage in said well by passing a prescribed current in a forward direction into a diode 315a formed from said well and said source electrode of said MISFET.

Referring to **claim 10**, the '534 patent further discloses that the body biasing circuit 320 includes a current source (also) 320 provided between a first power supply line "common power supply line" or Vcc and a contact region of said well, and passes said prescribed current into said diode via said contact region.

Referring to **claim 11**, the '534 patent further discloses that said current source 320 generates said prescribed current using said first power supply line "common power supply line" or Vcc as a power supply source.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 2-9, 15-26, and 30** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '534 patent for being obvious.

Referring to **claim 16**, the '534 patent discloses a semiconductor integrated circuit device comprising a second MISFET 310 and a second body biasing circuit 320 as claimed and as detailed above, but fails to explicitly disclose a first MISFET and fails to disclose a first body biasing circuit. However, the reference discloses in column 5, lines 30+ that "[W]hile in the description above current source 320 provides a bias to transistor 310, for alternative embodiments in accordance with this invention current source 320 provides a bias to multiple transistors" and in column 7, lines 11-16, that the transistors could be PMOS or NMOS. Therefore, it is within the disclosure that the semiconductor integrated circuit device comprises a first MISFET. What is not apparent in the '534 patent's device is the first body biasing circuit. Nevertheless, one of ordinary skill in the art would recognize that if the first MISFET and the second MISFET are of opposite polarity (one is a PMOS and the other NMOS transistor), then all corresponding polarities of each transistor's components would need to be reversed, including the respective polarities of the body biasing circuit portions. Hence, the modified circuit of the '534 patent, a circuit with multiple transistors, one of which is a PMOS and another of which is an NMOS, would include a first body biasing circuit, and the source and drain of the first MISFET (the NMOS) would be formed in a first well of a second conductivity type and this first body biasing circuit would generate a voltage in the first well by passing a prescribed current in a forward direction into a diode formed from the first well and the source electrode of said first MISFET.

Referring to **claims 25 and 26**, the second body biasing circuit 320 of the modified circuit of the '534 patent further includes a second current source also labeled as 320 provided between a second power supply line and a contact region of said second well, and passes said prescribed current into said second diode 315a via said contact region of said second well. As mentioned above, the modified circuit would include the first body biasing circuit, which would include a first current source provided between a first power supply line and a contact region of the first well, and passes a prescribed current into said first diode 315a via said contact region of said first well.

Regard **claims 2-9 and 17-24**, although the '534 patent does not articulate all possible applications for the semiconductor integrated circuit device as claimed, it is within the skill of one in the art at the time the invention was made to modify the circuit of the '534 patent to include elements as claimed. For example, it is within the skill of one in the art at the time the invention was made to change the circuit of the '534 patent to comprise a plurality of circuit blocks wherein each circuit block comprises a body biasing circuit 320, and it is within the skill of one in the art at the time the invention was made to provide a power control unit for each circuit block. These changes do not result in any phenomenal consequence and therefor would have been obvious to one of ordinary skill in the art.

Regard **claims 15 and 30**, although the '534 patent does not disclose a mode of operation as claimed, it appears that the '534 patent's circuit, which is similar in the claimed structure, could function as claimed.

Allowable Subject Matter

5. **Claims 12, 14, 27, 29**, and respective dependent claims 13 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor integrated circuit device having all exclusive limitations as recited in claims 1/10/11/12 (claims 1, 10, 11, and 12), 1/10/11/14, 16/25/26/27, and 16/25/26/29, characterized in the circuits of claims 12 and 14 respectively.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,469,572 to Bruneau et al. discloses a forward body bias generation circuit based on a diode clamp, a current mirror portion, an amplifier, and a current source.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
June 07, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800